Pinhole formation in solid phase epitaxial film of $CoSi_2$ on Si(111)

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The long-standing pinhole problem in solid phase epitaxial growth of a $CoSi_2$ film on Si(111) has been revisited with *in situ* scanning tunneling microscopy. While the as-deposited film with 5 Å of Co at room temperature shows a smooth granular texture with original substrate terraces remaining intact, annealing at 580 °C produces an epitaxial $CoSi_2$ film with large pinholes enclosed by a thin ring $CoSi_2$, exhibiting a volcano feature. Quantitative analysis shows that the formation of pinholes is a result of rapid Si outward diffusion from bulk to surface, and of the subsequent Si reaction with Co on the outer surface. Evidence suggests that inhibiting the Si diffusion channels during the thermal annealing process is the key to solving the pinhole problem. © *1998 American Institute of Physics.* [S0003-6951(98)03926-6]

Owing to its low resistivity and good epitaxial alignment with a Si substrate, $CoSi_2$ has emerged as a leading choice of the contacting material in future generation Si devices.[1] So far, however, $CoSi_2$ has failed to find wide application due to the lack of integrable fabrication procedures necessary to achieve a high quality film. One of the major difficulties is the unavoidable presence of sizable pinholes in $CoSi_2$ films, produced by molecular beam epitaxy (MBE) or by solid phase epitaxy (SPE),[2] which can lead to a undesirable large current leakage and ultimately to the device failure. This problem is even more fatal as the dimension of devices continues to shrink. Considerable efforts have been devoted to solve the pinhole problem by various deposition and reaction schemes but only limited success has been achieved in laboratories.[3–8] Although smooth silicide film could be obtained via a precise control of co-deposition of Co and Si at room temperature (RT) or at 400 °C,[7] large pinholes inevitably appear following a subsequent annealing near 600 °C, which is a mandatory step to improve the electrical conductivity. Pinhole-free $CoSi_2$ film has reportedly been obtained in mesotaxy using high energy and high dose ion implantation,[9] but this method requires dedicated tools which are not practical in conventional Si processing. More recently, a number of template mediated growth methods, such as using Ti or oxide as an interlayer, have shown promising results for a pinhole-free $CoSi_2$ fabrication procedure.[8,10]

Despite being a long-standing problem, the true origin of the pinhole formation in $CoSi_2$ has not yet been satisfactorily established. Surface and interface energies are the most common source of reasoning by many authors since the formation of pinholes could be the easiest kinetic pathway to reach a reduction of surface and interface energies.[2] Experimental findings are, however, much less in unison. Early on, this problem was described as a dewetting process driven by either a smaller surface energy for the Si(111) than for $CoSi_2$ or by a high interface energy.[11] But this simple model is inconsistent, respectively, with the fact that Si islands tend to form on $CoSi_2$ (Ref. 3) and that $CoSi_2$ layers with a Si rich surface exhibit good thermal stability.[6] The relief of the misfit stress in the $CoSi_2$ layers had also been sought as the reason behind the pinhole formation.[4] Measurements of the lattice parameters with and without a high density of pinholes, however, showed that pinholes have no effect on the film strain.[5] SPE-grown $CoSi_2$ often contains a fraction of type-A orientation as intermediate phases.[4] The idea that the conversion of type-A into type-B grains could be related to the pinhole formation was thus proposed,[12] but only to be abandoned shortly after since even in SPE-grown single crystal $CoSi_2$, pinholes were found to be unavoidable. By carefully controlling the deposition, the surface of $CoSi_2$ can be made to have a $CoSi_2$-C (Co rich) or a $CoSi_2$-S (Si rich) structure, with the latter being a more stable one against thermal annealing. It was found that the transformation from the former to the latter is accompanied by the pinhole formation. Therefore the energetic difference between these two phases was identified as the responsible factor for the pinhole problem.[6,7] This latest idea has also been challenged by a scanning tunneling microscopy (STM) study showing pinholes occur even on an initially Si-rich film upon annealing.[7] Furthermore, it may also be questioned why the segregation of Si must be achieved through delivery from pinholes rather than bulk diffusion in view of a recent experiment which has shown that Co diffusion in bulk Si far surpasses that on its surface.[13] In short, conflicting findings seem to exist for every mechanism proposed so far. It is clear that energetic consideration alone cannot account for the diverse experimental data, and a more adequate model must also include the detailed role of the kinetics involved.

In an attempt to obtain the microscopic origin of the pinhole formation, we have carried out an *in situ* study of SPE growth of $CoSi_2$ on Si(111), using STM to reveal the surface morphology associated with the deposition and silicidation procedures. In this letter we present direct evidence showing that the pinhole formation is a consequence of Si outward diffusion from bulk to surface and the subsequent Si reaction with Co on the outer surface to form a ring of $CoSi_2$ around the pinhole. This observation suggests that attention should be shifted towards the understanding of the origin and introduction of the diffusion channels during thermal processing. Inhibiting these channels could hold the key to a successful prevention of the pinhole problem.

The experiments were carried out in an ultrahigh

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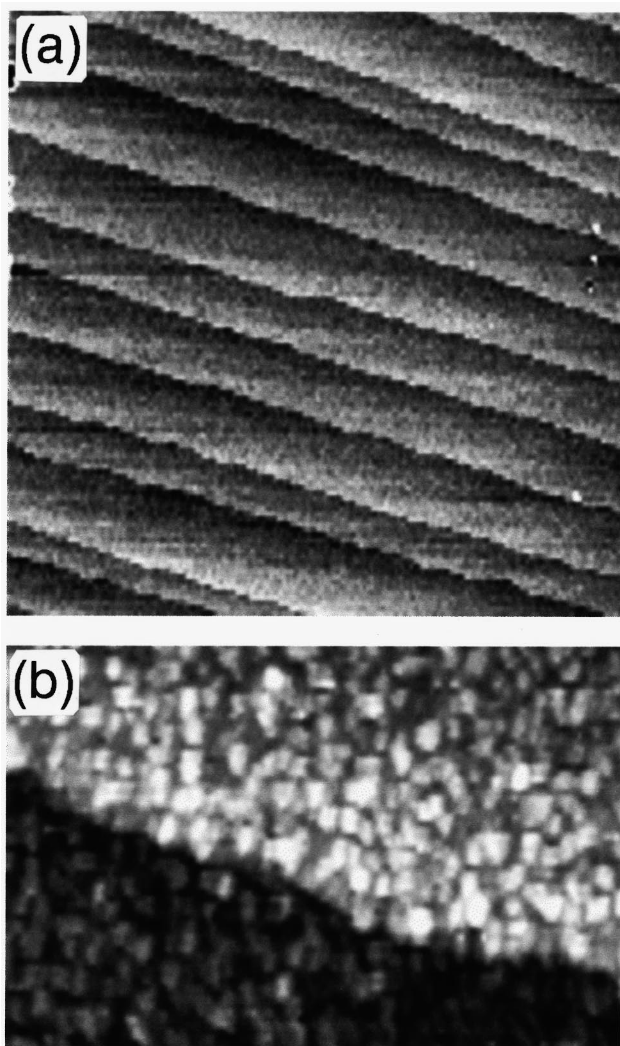

FIG. 1. (a) A 1.5 μm×1.5 μm STM image of 5 Å Co deposited on Si(111) at RT. (b) A higher resolution scan (770 Å×5000 Å) showing a granular texture of the surface with a vertical corrugation of ~2.5 Å. The lateral grain size varies from 20 to 30 Å.

vacuum (UHV) system equipped with a homemade scanning tunneling microscope (STM), a low energy electron diffraction (LEED) unit, and a cylindrical mirror analyzer for Auger electron spectroscopy (AES). With a vacuum base pressure of 7×10^{-11} Torr, a clean Si(111)(7×7) surface was routinely obtained on a piece of *n*-type Si(111) wafer (0.05 Ω·cm) by annealing at 1100–1200 °C. While the substrate was kept at room temperature, Co was deposited at a rate of ~2.5 Å/min from a tungsten boat heated at ~900 °C. The Co coverage was determined from the AES data, which in turn was calibrated against *ex situ* Rutherford back scattering (RBS) measurements. The $CoSi_2$ phase was obtained by postdeposition annealing to 580 °C for 2 min via passing a current through a piece of 5-μm-thick Ta foil on the back side of the silicon wafer. We have studied Co coverage from 2 to 15 Å [1 Å Co=1.17 monolayer (ML), or 9.1×10^{14} atoms/cm^2], but only the low coverage result will be presented as it enables the most unambiguous interpretation.

Figure 1 shows two STM images of the surface morphology of 5 Å Co deposited on a Si(111) sample at RT. The large-scale image of Fig. 1(a) (1.5 μm×1.5 μm) shows that the steps descending from upper right to the lower left are running along the original orientation of the bare substrate with the same straightness. Higher resolution scans such as those shown in Fig. 1(b) reveal that the terraces have a uniform and smooth granular texture. The averaged grain is 2.5 Å high and 25 Å wide. Auger measurements show that our sample contains a Co rich mixture with about 30% content of Si near the surface as a result of the RT reaction. These results are consistent with earlier reports on RT Co deposition. Both ultraviolet (UV) and x-ray photoemission experiments[14,15] showed that below 4 ML Co will react with Si even at room temperature and produce a mixture of CoSi and $CoSi_2$,[14,15] which is poorly ordered according to x-ray standing wave measurement,[16] but higher Co coverage yielded an excess metallic Co film on top. Our STM images clearly indicate that the RT Co–Si reaction takes place only locally and no long-range mass transport occurs by either species.

Annealing the as-deposited sample at 580 °C yields an epitaxial $CoSi_2$ film which give rises to a sharp (1×1) LEED pattern. Figure 2 shows the typical STM images of the annealed sample. Two important features are quite visible in these images. First, a larger number of randomly distributed deep voids (dark patches) appear in the sample [Fig. 2(a)]. These are the well-known pinholes. The opening of the pinholes ranges from 500 to 1500 Å and the depth varies from 20 to 50 Å, surpassing the $CoSi_2$/Si interface roughly 20 Å below the surface in agreement with the earlier STM study.[7] Second, apart from these pinholes, the granular texture in the as-deposited sample is now replaced with atomically flat terraces. The 5 Å Co deposition should yield ~20 Å of $CoSi_2$. It is quite remarkable that there is no significant increase in the step meandering or change in the step density after annealing. A step morphology resembling that of the substrate has been observed in transverse-electromagnetic mode (TEM) images of a $CoSi_2$ film grown by predeposition of a few angstroms of Co followed by the co-deposition of disilicide as required by the symmetry.[17] The preservation of the original substrate step morphology in the $CoSi_2$ film was attributed to limited lateral diffusion at RT.[18]

Quite notably, higher resolution STM images, such as seen in Fig. 2(b), further reveal that many of the pinholes are each fully or partially enclosed by an elevated bank of $CoSi_2$, 3–11 Å high and 500–1000 Å wide. The distinct volcano feature of the pinhole indicates a strong correlation between the Si atoms that are removed from the pinhole and its surrounding $CoSi_2$ islands. To understand the underlying relationship, we compare the volume of pinholes, $V_{\rm hole}$, with that of its surrounding islands, $V_{\rm island}$. We measure the height of the islands and the depth of the pinhole with respect to the nearby flat terraces and approximate the pinhole with straight walls. To minimize the errors, we only use pinholes with an opening sufficiently large to allow the tip to reach its bottom. Figure 3 plots $V_{\rm island}$ against $V_{\rm hole}$, for 18 isolated holes in two different samples, and the straight line is a least square fit to the data. It shows that within the accuracy of our measurement, $V_{\rm island}/V_{\rm hole}$ is essentially a constant and equal to 0.9. It follows from the atomic densities of the reactants that, for a given quantity of Si, the relative volume between $CoSi_2$ and Si is $V_{CoSi_2}/V_{Si}=0.84$, i.e., to grow 32 Å of $CoSi_2$ one needs to consume 10 Å of Co and

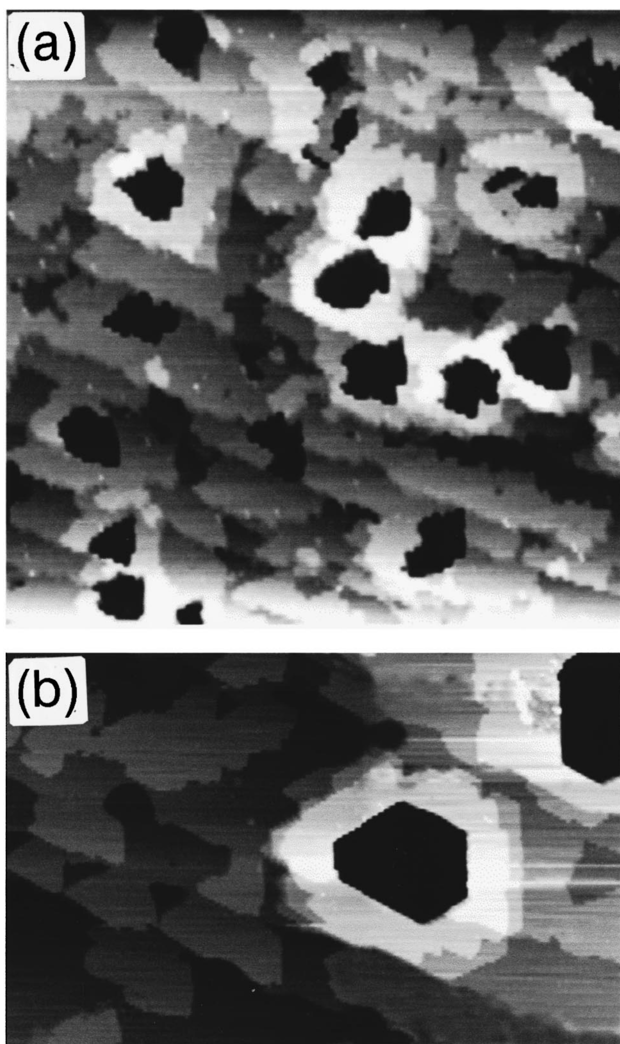

FIG. 2. (a) A 1.5 μm×1.5 μm STM image of a 20 $CoSi_2$ on Si(111) obtained by post-room-temperature-deposition annealing at 580 °C. The Co coverage is ~5 Å. The depth of the pinholes (dark patches) varies from 20 to 50 Å while the opening ranges between 400 and 1500 Å. (b) A 8500 Å ×5500 Å STM image of a pinhole enclosed by a elevated bank of $CoSi_2$, forming a volcanolike feature.

38 Å of Si. From the comparison of theoretical value of V_{CoSi_2}/V_{Si} with the measurement of V_{island}/V_{hole}, we conclude that the Si atoms excavated from the pinholes are responsible for building up its surrounding $CoSi_2$ ring. The small discrepancy may reflect the inability of the STM to obtain a precise dimension and shape of the pinholes.

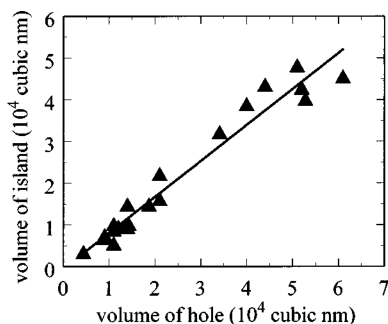

FIG. 3. The correlation between the volume of pinholes and the volume of the respective surrounding islands. The solid line is a least square fit to the data in filled triangles. A ratio of ~0.9 indicates that Si atoms removed from pinhole are consumed in the surrounding island.

Based on our STM results and the above quantitative analysis, we postulate that during the postdeposition annealing some diffusion channels are activated to expose the Si substrate, permitting a significant mass transport from bulk Si to the surface. The arriving Si atoms react with Co atoms from the outer surface to form a $CoSi_2$ ring, in vigorous competition with the silicidation process occurring at the buried interface, and thus giving rise to the volcano feature of the pinholes [Fig. 2(b)]. In general, the surface morphology depends strongly on the Co coverage and the annealing temperature. At lower coverage, pinhole generated islands do not form an enclosure while at high coverage the islands associated with neighboring pinholes are coalesced, both making it difficult to identify the unique process described here.

The driving force for the Si outward diffusion is clearly due to the free Co atoms on the outer surface. However, diffusion channels would have to be activated to allow the Si atoms to rush to the surface in mass, which results in the pinhole morphology. This is a rapid thermal process and cannot be studied by our present setup. Nonetheless, our result suggests that inhibiting these diffusion channels through some means may very well be a more effective way to eliminate pinholes in $CoSi_2$ processing. Indeed, we speculate that this could be the main reason behind several successful fabrication schemes such as the interrupted co-deposition and the template mediated growth, all yielding a $CoSi_2$ film with little or no pinholes. Detailed *in situ* microscopic characterization and especially real time studies of the growth kinetics may help to bring this long-standing problem to a close.

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